

CLAIMS

What is claimed is:

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1. A multi-stage, multi-dimensional, credit-based, adaptive flow control switch comprising:

10 a plurality of first stage port processors, each one of the plurality of first stage port processors having an integrator block for receiving a token bit and updating a grant credit in response to receiving the token bit; and

15 a plurality of second stage port processors connected to the plurality of first stage port processors for receiving data packets from the plurality of first stage port processors, each one of the plurality of second stage port processors having a statistics block coupled to a corresponding integrator block;

20 the statistics block further coupled to one or more neighboring integrator blocks for transmitting a token bit to the corresponding integrator block and the one or more neighboring integrator blocks, the statistics block transmitting the token bit in response to a second stage port processor associated with the statistics block receiving a data packet from one of the plurality of the first stage port processors.

2. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 1, wherein the corresponding integrator block includes an (i)th integrator block and the one or more neighboring integrator blocks include an (i-1)th integrator block that is located above the corresponding (i)th integrator block.

3. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 2, wherein

the one or more neighboring integrator blocks further include an (i+1)th integrator block that is located below the corresponding (i)th integrator block.

5       4. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 3, wherein the one or more neighboring integrator blocks increase associated grant credits in response to receiving a token bit from the statistic block.

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15       5. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 4, wherein the corresponding integrator block decreases an associated grant credit in response to receiving a token bit from the statistic block.

20       6. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 5, wherein the plurality of first stage port processors includes one or more input ports and one or more output ports, wherein the arriving data packet is received at one of the one or more input ports and routed to an output port having a maximum number of grant credit.

25       7. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 1, wherein the switch further includes:

30              a plurality of third stage port processors connected to the plurality of second stage port processors; and

35              the statistic block further includes a real-time counter for accumulating real-time statistics of data packet arrivals from one of the plurality of first stage port processors and data packet departures to one of the plurality of third stage port processors.

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8. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 7, wherein the switch further includes a relay from each one of the third stage port processors to the plurality of first stage port processors, and the token bit is transmitted to the first stage port processors by one of second stage port processor and the third stage port processor.

9. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 8, wherein the plurality of first stage switch elements and the plurality of third stage switch elements are embedded on a single chip.

15 10. An adaptive filtering method for controlling traffic flow in a multi-stage, multi-dimensional, switched network, comprising:

20 notifying a plurality of first stage port processors in response to receiving a data packet from one of the plurality of first stage port processors; and

25 updating grant credits associated with said one of the plurality of first stage port processors and one or more neighboring first stage port processors in response to the notifying.

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11. The adaptive filtering method of claim 10, wherein the notifying includes:

20 notifying said one of the plurality of first stage port processors; and

30 notifying said one or more neighboring first stage port processors.

35 12. The adaptive filtering method of claim 11, wherein the updating grant credits includes:

decrementing a grant credit associated with said one

of the plurality of first stage port processors; and  
incrementing one or more grant credits associated  
respectively with the one or more neighboring first stage  
port processors.

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13. The adaptive filtering method of claim 12,  
further including:

determining a port processor among the plurality of  
first stage port processors for forwarding an incoming data  
10 packet by selecting an output port processor having a  
maximum grant credit.

14. The adaptive filtering method of claim 13,  
further including:

15 receiving the incoming data packet at the determined  
port processor; and

routing the data packet to a corresponding second  
stage port processor.

20 15. The adaptive filtering method of claim 10,  
wherein the one or more neighboring first stage port  
processors include a first stage port processor coupled  
adjacent to said one of the plurality of first stage port  
processors.

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16. The multi-stage, multi-dimensional, credit-based,  
adaptive flow control switch as claimed in claim 1, wherein  
the one or more neighboring integrator blocks change  
associated grant credits in response to receiving a token  
30 bit from the statistic block.

17. The multi-stage, multi-dimensional, credit-based,  
adaptive flow control switch as claimed in claim 1, wherein  
the corresponding integrator block change an associated  
35 grant credit in response to receiving a token bit from the

statistic block.

18. The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 1, wherein  
5 the statistics block departs the data packet.

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